The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BRENT KEETH

Appeal No. 2000-1599
Application No. 08/798,227

ON BRIEF

Before THOMAS, LALL, and LEVY, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellant has appealed to the Board from the examiner's final rejection of claims 1 through 24.

Representative claim 1 is reproduced below:

1. A method of adjusting data timing in a memory system having a memory device and a memory controller, the system operating according to a master clock signal, the method comprising the steps of:

establishing an initial output timing at the memory device;

transmitting an echo clock signal from the memory device to the memory controller according to the initial output timing;

receiving the echo clock signal at the memory controller;

identifying a phase error of the received echo clock signal relative to the master clock signal;

transmitting control data from the memory controller to the memory device for revising the initial output timing in response to the identified phase error to produce a revised output timing;

revising the initial output timing at the memory device according to the control data; and

transmitting a second set of data from the memory device to the memory controller according to the revised output timing.

The following references are relied on by the examiner:

Smith	5,020,023	May 28, 1991
Johnson et al. (Johnson)	5,577,236	Nov. 19, 1996

Claims 1 through 6, 8 through 11, 13 through 18 and 20 through 24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Johnson. The remaining claims on appeal, claims 7, 12 and 19 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Johnson in view of Smith.

Rather than repeat the positions of the appellant and the examiner, reference is made to the brief and the answer for the respective details thereof.

OPINION

Because our study of Johnson leads us to agree with appellant's position set forth at pages 7 and 9 of the brief on appeal, we reverse the rejection of all earlier-noted claims under 35 U.S.C. § 102 and, consequently, the additional rejection of certain claims under 35 U.S.C. § 103. The rejection under 35 U.S.C. § 102 encompasses each of the independent claims 1, 6, 10, 13, 16 and 20 on appeal. For the following reasons, we reverse the rejection of each of them as being anticipated by Johnson.

Since appellant considers claim 20 to be representative of the subject matter of claims 1, 6, 16 and 20, we agree with the arguments presented by the appellant at page 7 of the brief:

> Claim 20 specifies a method of adjusting data timing in a memory system having a memory device and a memory controller. According to the claimed method, an initial output timing at the memory device is established and is then subsequently revised. The output timing is revised by "transmitting a first digital signal from the memory device to the memory controller according to the initial output timing." After the echo clock signal is received at the memory controller, the memory controller identifies "a phase difference of the received echo clock signal relative to a

> timing reference signal" and "transmits an adjustment signal to the memory device for revising the initial output timing in response to the identified phase difference to produce a revised output timing." Thereafter, the memory device revises the initial output timing according to the adjustment signal. The memory device then transmits a second digital signal from the memory device to the memory controller according to the revised output timing.
>
> As explained above, the Johnson et al. patent does not disclose a memory controller that identifies a phase error between a received digital signal relative to a timing reference signal, as recited claim 20. Nor does the Johnson et al. system transmit an adjustment signal to the memory device to cause the memory device to revise the initial output timing. Finally, the Johnson et al. patent does not disclose any system in which the timing of a signal generated by a memory device can be adjusted. Instead, the only signal having its timing adjusted in the Johnson et al. system is selecting one of several sampling clock signals, but this selection is done in the memory controller and not in the memory device, as in applicant's system.

Corresponding limitations are set forth as noted in the last paragraph with respect to claim 20 in independent claims 1, 6 and 16 on appeal. As to independent claim 1, this claim requires in part the identification of a phase error of a received echo clock signal sent by the memory device relative to the master clock signal, and subsequently transmitting control data from the memory controller to the memory device to produce a revised output timing in the memory device according to the control data. As to independent claim 6, this claim in part requires the production of an echo signal at the memory device, which signal

is transmitted to the memory controller which receives it and compares it with the master clock signal. Thereupon, the memory controller selects an adjusted time delay in response to this comparing step. Another read command is issued to the memory device which, in turn, transmits to the memory controller a second set of data with the adjusted time delay. Turning to independent claim 16, this claim in part recites the establishment of an initial output timing at the memory device having a default phase relationship with the first clock signal. Thereupon, the memory device transmits a second set of data to the memory controller, which in turns receives it and compares this second set of data to a first clock control signal in order to identify a phase error. This identified phase error is used in the memory controller to issue a revised initial timing signal which is received at the memory device to revise its output timing.

To the extent the memory device RAM of prior art Figure 1 in Johnson is utilized for the memory modules 300a-d in Figure 3, it is apparent that there is no circuitry disclosed therein which reacts to any commands sent by the memory controller 302 in Figure 3 to change the memory module's timing as required in some manner by each of these independent claims on appeal.

As to the remaining independent claims 10 and 13 on appeal we agree with the appellant's arguments presented at page 9 of the brief as to representative claim 10 of these two claims:

> The Johnson system does not anticipate the subject matter of claim 10. More specifically, the Johnson system does not have a phase comparing circuit which compares the phase difference between a signal transmitted by the memory device and a clock signal of the memory controller. The system shown in Figure 3 and described in col. 5, line 19-col. 7, line 40 does not include a phase comparing circuit that compares the phase error between a clock signal transmitted from the memory bank to the memory controller or a logic circuit that produces a signal in response to the output of the phase comparing circuit.

Although the focus of the subject matter of the body of independent claim 10 on appeal is the details of a memory controller, the preamble of claim 10 recites the memory device producing echo signals. The body of claim 10 therefore recites a phase comparing signal which determines the phase difference between these received echo signals and the master clock signal

in the memory controller, which comparison causes a logic circuit within the memory controller to produce an adjustment data in response to this phase signal. As noted by appellant in the just-quoted material in the preceding paragraph, the teachings and showings in Figure 3 of Johnson are not capable of meeting these noted requirements of claim 10 on appeal. Finally, as to independent claim 13, for reasons which we have stated earlier in this opinion, the detailed circuit elements recited as to the memory device itself in claim 13 cannot be met by Johnson because there are no details of the memory devices' elements and functions thereof in Johnson to meet the limitations of the memory device clause of claim 13 on appeal.

Since we do not sustain the rejection of any of the independent claims 1, 6, 10, 13, 16 and 20 on appeal under 35 U.S.C. § 102, we do not sustain the rejection of any of their respective dependent claims and, consequently, the rejection of certain of their dependent claims under 35 U.S.C. § 103, further in view of Smith.

Therefore, the decision of the examiner rejecting the claims on appeal under 35 U.S.C. § 102 and 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)
Administrative Patent Judge)
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PARSHOTAM S. LALL) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
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STUART S. LEVY)
Administrative Patent Judge)

JDT:hh

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EDWARD W. BULCHIS, ESQ.
DORSEY AND WHITNEY, LLP
U.S. BANK CENTRE, STE. 3400
1420 FIFTH AVE.
SEATTLE, WA 98101